UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|---|---|---|---|
| 10/828,463 | 04/21/2004 | Kyoung-Ho Kang | 61610139US | 5334 |

58027 7590 10/16/2007

H.C. PARK & ASSOCIATES, PLC
8500 LEESBURG PIKE
SUITE 7500
VIENNA, VA 22182

| EXAMINER | |
|---|---|
| PERVAN, MICHAEL | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2629 | |

| NOTIFICATION DATE | DELIVERY MODE |
|---|---|
| 10/16/2007 | ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

PATENT@PARK-LAW.COM

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/828,463 | KANG ET AL. | |
| | Examiner | Art Unit | |
| | Michael Pervan | 2629 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *20 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 April 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *9/20/07*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

## DETAILED ACTION

### *Claim Rejections - 35 USC § 103*

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-3, 8-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al (US 6,262,699) in view of Awamoto et al (US 6,525,486).

In regards to claim 1, Suzuki discloses a driver for driving a plasma display panel (col. 4, lines 54-56), wherein the plasma display panel includes a plurality of address electrodes (Fig. 3), a plurality of X electrodes (Fig. 3) and a plurality of Y electrodes (Fig. 3), said driver comprising:

an address driver (Fig. 3 and col. 5, lines 32-36);

an X driver (Fig. 3 and col. 5, lines 11-14); and

a Y driver (Fig. 3 and col. 5, lines 5-11),

wherein the plurality of X electrodes and the plurality of Y electrodes are arranged alternately next to each other forming a XY electrode pair group and in substantially perpendicular to the to the plurality of address electrodes (Fig. 3; as can be seen from the drawing the X and Y electrodes alternate and form XY electrode pairs which are perpendicular to the plurality of address electrodes),

wherein the XY electrode pairs are divided into a plurality of XY electrode pair groups (Fig. 3; as can be seen from the drawing the XY electrode pairs are divided into a plurality of XY electrode groups), and

wherein at least one of the X driver and the Y driver comprises a plurality of driving circuits, each driving circuit corresponding to one of the plurality of XY electrode pair groups (Fig. 3; as can be seen from the drawing the Y driver comprises a plurality of driving circuits).

Suzuki does not disclose driving circuits commonly connected to a reset circuit.

Awamoto discloses driving circuits commonly connected to a reset circuit (Fig. 7 and col. 7, line 62-col. 8, line 7; driving circuits (scan drivers 781) are commonly connected to a reset circuit (reset voltage circuit 782, 783)).

It would have been obvious at the time of invention to modify Suzuki with the teachings of Awamoto, driving circuits commonly connected to a reset circuit, because it would ensure that the reset is applied to all of the electrodes at the same time.

In regards to claim 2, Suzuki discloses the driver of claim 1, wherein the plurality of driving circuits operate independently to perform an addressing operation and a display sustain discharge operation alternately (Figs. 4C-I; as can be seen from the drawings electrodes $Y_1$-$Y_n$ are independent and alternate addressing and sustain) and to apply a voltage for display-sustain discharge only to an XY electrode pair group that has already been addressed (Figs. 4C-4I; as can be seen from the drawings the sustain voltage is applied after the addressing period).

In regards to claim 3, Suzuki discloses the driver of claim 1, wherein each of the plurality of driving circuits of the Y driver comprises:

a scan circuit (a circuit which provides a scan pulse) that sequentially applies a scan pulse to the plurality of Y electrodes for addressing (Fig. 4 and col. 5, lines 48-65; the Y drivers provide a scan pulse, therefore a scan circuit must be present); and

a sustain circuit (a circuit which provides a sustain pulse) that simultaneously applies periodical display-sustain pulses of the alternating current voltage to the plurality of Y electrodes (Fig. 4 and col. 6, lines 51-58; the Y driver provides a sustain pulse, therefore a sustain circuit must be present).

In regards to claim 8, Suzuki does not disclose the driver of claim 3, wherein the reset circuit is arranged in the Y driver and performs a reset operation for having a state of charges in every display cell uniform.

Awamoto discloses the reset circuit is arranged in the Y driver and performs a reset operation for having a state of charges in every display cell uniform (Fig. 7 and col. 7, line 62-col. 8, line 7; the reset circuit (reset voltage circuit 782, 783) is arranged in the Y driver).

It would have been obvious at the time of invention to modify Suzuki with the teachings of Awamoto, reset circuit arranged in the Y driver and performs a reset operation, because by having all of the components, reset circuit and driving circuits, in one single component, it makes manufacturing and repairs easier since there is one component instead of multiple.

In regards to claim 9, Suzuki discloses the driver of claim 8, wherein the X driver comprises a single reset circuit (a circuit which provides a reset pulse) that operates together with the reset circuit of the Y driver (col. 5, lines 15-26; the X driver provides a reset pulse, therefore there must be a reset circuit present).

In regards to claim 10, Suzuki discloses the driver of claim 8, wherein each of the plurality of driving circuits of the X driver comprises a sustain circuit (a circuit which provides a sustain pulse) which simultaneously applies periodical display-sustain pulses of the alternating current voltage to the X electrode lines (Fig. 4 and col. 6, lines 51-58; the X driver provides a sustain pulse, therefore a sustain circuit must be present).

3. Claims 4-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al in view of Awamoto et al in further view of Lee et al (US 2003/0057858).

In regards to claim 4, Suzuki and Awamoto disclose the driver of claim 3, wherein the scan circuit comprises:

a scan driving circuit (a circuit that provides a scan pulse) (Fig. 4 and col. 5, lines 48-65; the Y drivers provide a scan pulse, therefore a scan circuit must be present).

Suzuki and Awamoto do not disclose a switching output circuit.

Lee discloses a switching output circuit (Fig. 7).

It would have been obvious at the time of invention to modify Suzuki and Awamoto with the teachings of Lee, a switching output circuit, to improve display performance (paragraph 18).

In regards to claim 5, Suzuki and Awamoto do not disclose the driver of claim 4, wherein the switching output circuit comprises:

an upper transistor (Fig. 7; $YU_1$-$YU_n$);

a lower transistor (Fig. 7; $YL_1$-$YL_n$); and

a common output line for the upper transistor and the lower transistor (Fig. 7; $Y_1$-$Y_n$),

wherein the common output line is coupled to one of the plurality of Y electrodes (Fig. 7; $Y_1$-$Y_n$).

Lee discloses wherein the switching output circuit comprises an upper transistor, a lower transistor and a common output line for the upper transistor and the lower transistor, wherein the common output line is coupled to one of the plurality of Y electrodes.

It would have been obvious at the time of invention to modify Suzuki and Awamoto with the teachings of Lee, wherein the switching output circuit comprises an upper transistor, a lower transistor and a common output line for the upper transistor and the lower transistor, wherein the common output line is coupled to one of the plurality of Y electrodes, to improve display performance (paragraph 18).

In regards to claim 6, Suzuki and Awamoto do not disclose the driver of claim 5, wherein the scan circuit is coupled to an upper common power line of the upper transistor and to a lower common power line of the lower transistor to apply a scan voltage to one of the plurality of Y electrodes that is scanned during an addressing period and to apply a scan bias voltage to one of the plurality of Y electrodes that is not scanned during the addressing period.

Lee discloses the driver of claim 5, wherein the scan circuit is coupled to an upper common power line of the upper transistor and to a lower common power line of the lower transistor (Fig. 7) to apply a scan voltage to one of the plurality of Y electrodes that is scanned during an addressing period (Fig. 8) and to apply a scan bias voltage to one of the plurality of Y electrodes that is not scanned during the addressing period (Fig. 8; Sy1 applies a voltage after the scan period).

It would have been obvious at the time of invention to modify Suzuki and Awamoto with the teachings of Lee, wherein the scan circuit is coupled to an upper common power line of the upper transistor and to a lower common power line of the lower transistor to apply a scan voltage to one of the plurality of Y electrodes that is scanned during an addressing period and to apply a scan bias voltage to one of the plurality of Y electrodes that is not scanned during the addressing period, to improve display performance (paragraph 18).

In regards to claim 7, Suzuki and Awamoto do not disclose the driver of claim 6, wherein an output of the sustain circuit is applied to one of the upper common power line and the lower common power line via the scan driving circuit.

Lee discloses the driver of claim 6, wherein an output of the sustain circuit is applied to one of the upper common power line and the lower common power line via the scan driving circuit (Fig. 7; as can be seen from the drawing the sustain circuit ($SP_y$ is connected to the common power line of the upper transistor via the scan circuit).

It would have been obvious at the time of invention to modify Suzuki and Awamoto with the teachings of Lee, wherein an output of the sustain circuit is applied to

one of the upper common power line and the lower common power line via the scan driving circuit, to improve display performance (paragraph 18).

4. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Suzuki et al in view of Awamoto et al in further view of Hashimoto et al (US 6,091,380).

In regards to claim 11, Suzuki and Awamoto do not disclose the driver of claim 2, wherein each of the plurality of driving circuits of the Y driver drives Y electrodes of a corresponding XY electrode pair group, each of the plurality of driving circuits of the X driver drives X electrodes of a corresponding XY electrode pair group, wherein an XY electrode pair group including the plurality of Y electrodes driven by one among the plurality of driving circuits of the Y driver is not the same as an XY electrode pair group including the plurality of the X electrodes driven by one among the plurality of driving circuits of the X driver.

Hashimoto discloses the driver of claim 2, wherein each of the plurality of driving circuits of the Y driver drives Y electrodes of a corresponding XY electrode pair group (Fig. 2; as can be seen from the drawing, scanning circuit 13(1)-13(n) drive corresponding electrodes), each of the plurality of driving circuits of the X driver drives X electrodes of a corresponding XY electrode pair group (Fig. 2, as can be seen from the drawing, Y drivers 16a and 16b driver corresponding electrodes), wherein an XY electrode pair group including the plurality of Y electrodes driven by one among the plurality of driving circuits of the Y driver is not the same as an XY electrode pair group including the plurality of the X electrodes driven by one among the plurality of driving

circuits of the X driver (Fig. 2; as can be seen from the drawing, the scanning circuit 13(1) has a different X electrode driver than scanning circuit 13(n)).

It would have been obvious at the time of invention to modify Suzuki and Awamoto with the teachings of Hashimoto, XY pair group of one Y driver has a different X driver than the other Y driver, because it would reduce power consumption because the drivers are smaller due to having more than one to drive the electrodes.

5. Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee et al in view of Suzuki et al in further view of Awamoto et al.

In regards to claim 12, Lee discloses a plasma display panel device (Fig. 5 and paragraph 15), comprising:

a plasma display panel (Fig. 5 and paragraph 15);

a video processor (Fig. 5 and paragraph 15);

a logic controller (Fig. 5 and paragraph 15);

an X driver that controls a plurality of X electrodes (Fig. 5 and paragraph 15);

a Y driver that controls a plurality of Y electrodes (Fig. 5 and paragraph 15); and

an address driver that controls a plurality of address electrodes (Fig. 5 and paragraph 15),

Lee does not disclose wherein the plurality of Y electrodes and the plurality of X electrodes are arranged alternately next to each other forming XY electrode pairs, wherein the XY electrode pairs are divided into a plurality of XY electrode pair groups and at least one of the X driver and the Y driver comprises a plurality of driving circuits corresponding to the plurality of XY electrode pair groups.

Suzuki discloses wherein the plurality of Y electrodes and the plurality of X electrodes are arranged alternately next to each other forming XY electrode pairs (Fig. 3; as can be seen from the drawing the X and Y electrodes alternate and form XY electrode pairs), wherein the XY electrode pairs are divided into a plurality of XY electrode pair groups (Fig. 3; as can be seen from the drawing the XY electrode pairs are divided into a plurality of XY electrode groups) and at least one of the X driver and the Y driver comprises a plurality of driving circuits, each driving circuit corresponding to one of the plurality of XY electrode pair groups (Fig. 3; as can be seen from the drawing the Y driver comprises a plurality of driving circuits).

It would have been obvious at the time of invention to modify Lee with the teachings of Suzuki, at least one of the X driver and the Y driver comprises a plurality of driving circuits corresponding to the plurality of XY electrode pair groups, because it can reduce an address write cycle and also realize a stable highly-fine/high-quality display without erroneous discharge (col. 3, lines 46-48).

Lee and Suzuki do not disclose driving circuits commonly connected to a reset circuit.

Awamoto discloses driving circuits commonly connected to a reset circuit (Fig. 8 and col. 7, lines 15-26; driving circuits (scan drivers 781) are commonly connected to a reset circuit (reset voltage circuit 782, 783)).

It would have been obvious at the time of invention to modify Lee and Suzuki, with the teachings of Awamoto, driving circuits commonly connected to a reset circuit,

because it would ensure that the reset is applied to all of the electrodes at the same time.

***Response to Arguments***

6. Applicant's arguments with respect to claims 1-12 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael Pervan whose telephone number is (571) 272-0910. The examiner can normally be reached on Monday - Friday between 8am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

MVP
Oct. 3, 2007

AMR A. AWAD
SUPERVISORY PATENT EXAMINER